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DALLAS SEMICONDUCTOR

DS2118M
Ultra2 LVD/SE SCSI Terminator

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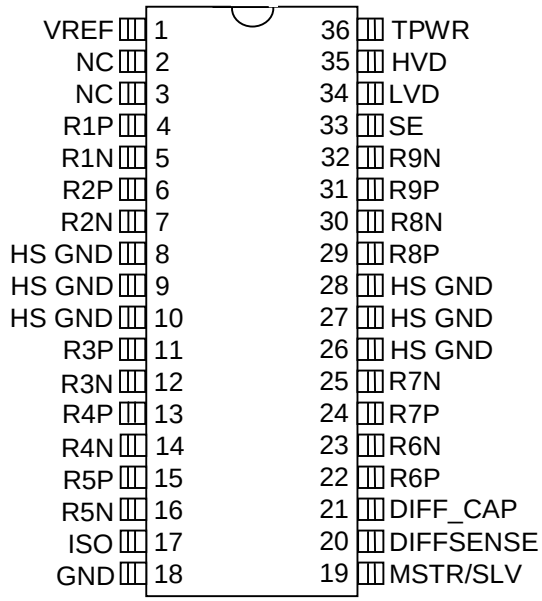
FEATURES

- Fully compliant with Ultra2 SCSI
- Provides Multimode Low Voltage Differential/Single-Ended (LVD/SE) termination for 9 signal line pairs
- Auto-selection of LVD or SE termination
- 5% tolerance on SE and LVD termination resistance
- Low power down capacitance of 3 pF
- Onboard thermal shutdown circuitry
- SCSI bus hot plug compatible
- Fully supports actively negated SE SCSI signals

PIN ASSIGNMENT



DS2118MB 36-Pin SSOP

DESCRIPTION

The DS2118M Ultra2 LVD/SE SCSI Terminator is both a Low Voltage Differential (LVD) and Single-Ended (SE) terminator. The multimode operation enables the designer to implement LVD in current products while allowing the end-user SE backward compatibility with legacy devices. If the device is connected in an LVD-only bus, the DS2118M will use LVD termination. If any SE devices are connected to the bus, the DS2118M will use SE termination. This is accomplished automatically inside the part by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2118M integrates two regulated supplies with nine precision resistor strings. For the SE termination, one regulator and nine precision 110-ohm resistors are used. Three DS2118M terminators are needed for a Wide SCSI bus.

REFERENCE DOCUMENTS

Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface (SPI) Project: 0855-M, 1995
Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface 2 (SPI-2) Project: 1142-M, 1998

Available from:
American National Standards Institute (ANSI) Phone: (212) 642-4900
Global Engineering Documents 15 Inverness Way East; Englewood, CO 80112 Phone: (800) 854-7179

FUNCTIONAL DESCRIPTION

The DS2118M combines LVD and SE termination with DIFFSENS sourcing and detection. The LVD termination section consists of two source/sink amplifiers (VTOP, VBOT), biasing circuitry and nine precision resistor strings (RTOP, RMID, RBOT). The SE termination section consists of a 2.85V source/sink regulator with 9 precision 110 Ohm resistors. The DIFFSENSE section consists of a 1.3V, 5 mA driver and a sensing circuit (Figure 1).

The DIFFSENSE circuitry decodes trinary logic. There will be one of three voltages on the SCSI control line called DIFFSENS. Two comparators and a NAND gate determine if the voltage is below 0.6V, above 2.15V, or in between. That indicates the mode of the bus to be HVD, SE, or LVD, respectively.

The DS2118M's DIFF_CAP pin monitors the DIFFSENS line to determine the proper operating mode of the device; this mode is indicated by the SE/LVD/HVD outputs. The DIFFSENSE pin can also drive the SCSI DIFFSENS line (when MSTR/SLV = 1) to determine the SCSI bus operating mode. The DS2118M switches to the termination mode that is appropriate for the bus based on the value of the DIFFSENS voltage. These modes are:

LVD mode LVD termination is provided by a precision laser trimmed resistor string with two amplifiers. This configuration yields a 105Ω differential and 150Ω common mode impedance. A fail-safe bias of 112 mV is maintained when no drivers are connected to the SCSI bus.

SE mode When the external driver for a given signal line turns off, the active terminator will pull that signal line to 2.85 volts (quiescent state). When used with an active negation driver, the power amp can sink 22 mA per line while keeping the voltage reference in regulation. The terminating resistors maintain their 110Ω value.

HVD Isolation Mode The DS2118M identifies that there is an HVD (high voltage differential) device on the SCSI bus and isolates the termination pins from the bus.

When ISO is pulled high, the termination pins are isolated from the SCSI bus, Vref remains active, and the bus mode indicators (SE/LVD/HVD) remain active. During thermal shutdown, the termination pins are isolated from the SCSI bus, Vref becomes high impedance, and the bus mode indicators (SE/LVD/HVD) remain active . The DIFFSENSE driver is shut down during either of these two events. An internal pull-down resistor assures that the DS2118M will be terminating the bus if the ISO pin is left floating.

To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and VDD lines should be bypassed locally. A 2.2 µF capacitor and a 0.01 µF high frequency capacitor is recommended between TPWR and ground and placed as close as possible to the DS2118M. The DS2118M should be placed as close as possible to the SCSI connector

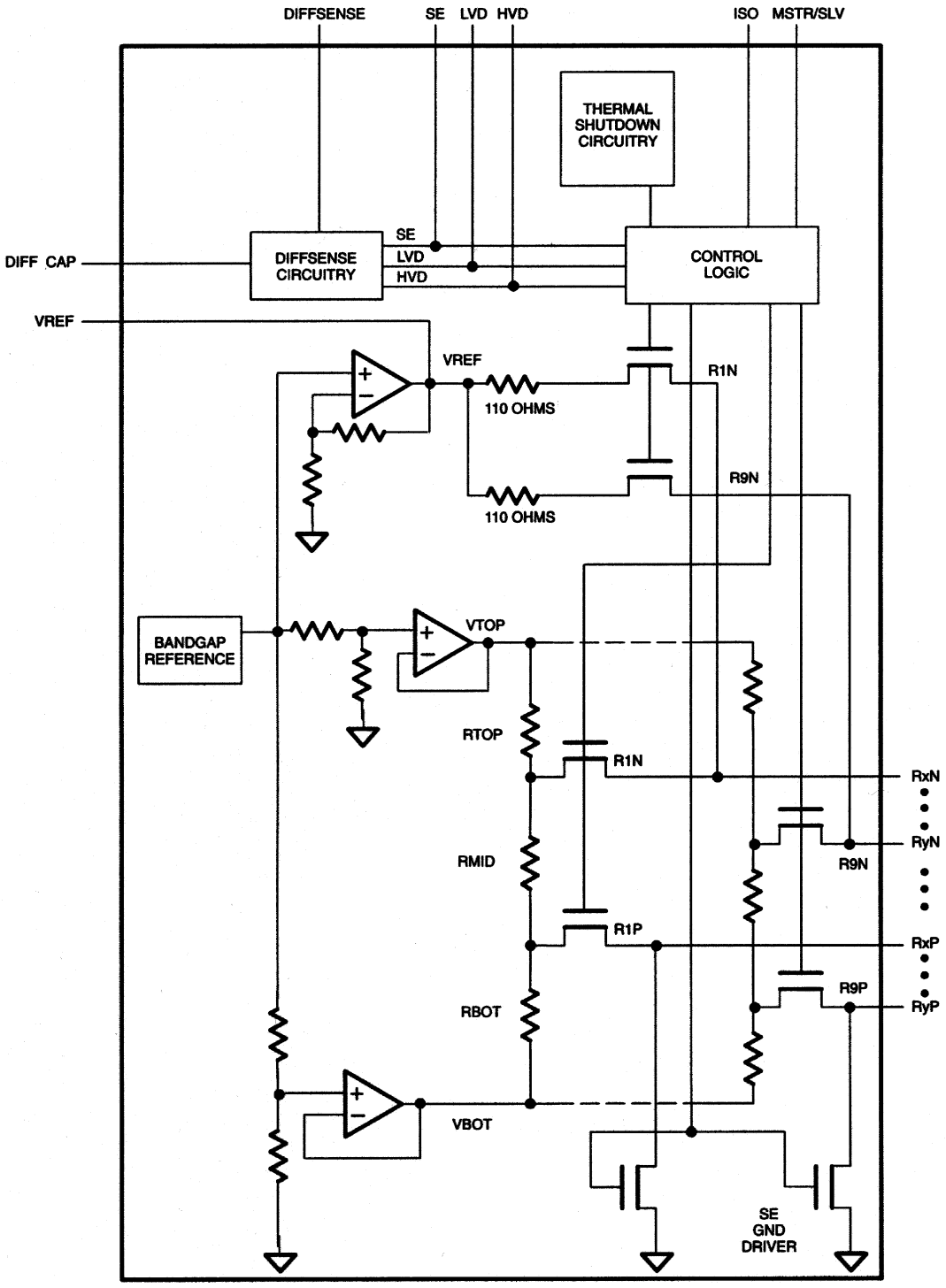
to minimize signal and power trace length, thereby resulting in less input capacitance and reflections which can degrade the bus signals.

To maintain the specified regulation, a 4.7 µF capacitor is required between the Vref pin (VREF) and ground of each DS2118M. A high frequency cap (0.1 µF ceramic recommended) can also be placed on the Vref pin in applications that use fast rise/fall time drivers. A typical SCSI bus configuration is shown in Figure 2.

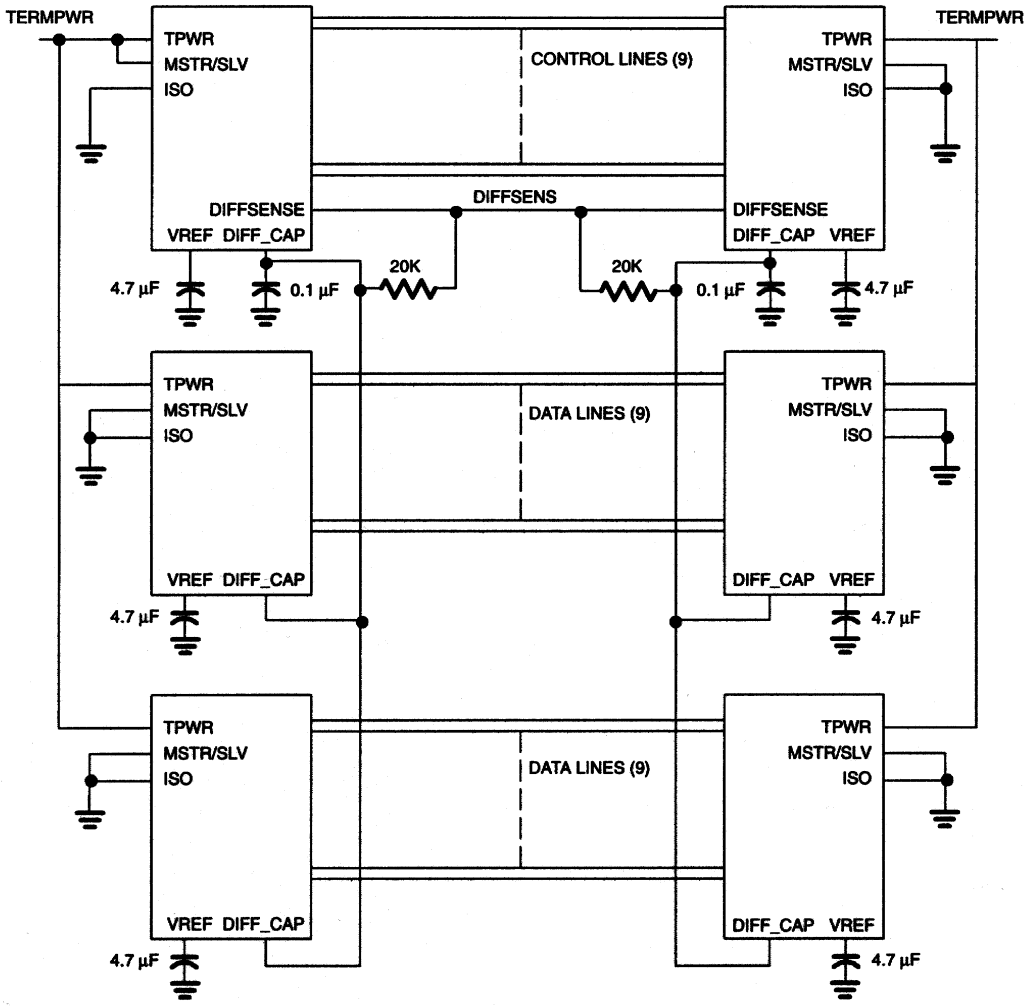
NOTE:

DIFFSENS – Refers to the SCSI bus signal.
DIFFSENSE – Refers to the DS2118M pin name and internal circuitry capable of driving the DIFFSENS line.
DIFF_CAP - Refers to the DS2118M pin name and internal circuitry relating to monitoring the DIFFSENS line.

DS2118M BLOCK DIAGRAM Figure 1



SCSI BUS CONFIGURATION Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	VREF	**Reference Voltage.** 2.85 volt reference; must be decoupled with a 4.7 µF cap.
2, 3	NC	**No Connect.** Do not connect these pins.
4-7, 11-16, 22-25, 29-32	RxP, RxN	**Signal Termination.** Connect to SCSI bus signal lines.
8, 10, 26, 9, 28, 27	HS GND	**Heat Sink Ground.** Internally connected to the mounting pad. Should be grounded.
17	ISO	**Isolation.** When pulled high, the DS2118M isolates it's bus pins (RxP, FxP) from the SCSI bus.
18	GND	**Ground.** Signal ground; 0.0 volts.
19	MSTR/SLV	**Master/slave.** Mode select for the non-controlling terminator. When pulled high (MSTR), the DIFFSENSE driver is enabled.
20	DIFFSENSE	**DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line.
21	DIFF_CAP	**DIFFSENSE CAPACITOR.** Connect 0.1 µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus.
33	SE	**Single-ended.** SE output of DIFFSENSE receiver; indicates SE bus operation.
34	LVD	**Low Voltage Differential.** LVD output of DIFFSENSE receiver; indicates LVD bus operation.
35	HVD	**High Voltage Differential.** HVD output of DIFFSENSE receiver; indicates HVD bus operation or thermal shutdown.
36	TPWR	**Termination Power.** Connect to the SCSI TERMPWR line and decouple with 2.2 µF capacitor.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Voltage	V_{tpwr}	4.0		5.50	V	
Logic 0	V_{il}	-0.3		+0.8	V	
Logic 1	V_{ih}	2.0		V_{tpwr} + 0.3	V	
Operating Temperature	V_{amb}	0		70	°C	

SINGLE ENDED CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SE Termination Resistance	Rse	104.5	110	115.5	Ohms	Vline=0-3.0 volts
SE Voltage Reference	Vref	2.79		2.93	Volts	
SE Output Current	lose			25.4	mA	Vline = 0.2 volts
Output Capacitance	Cout			3	pF	guaranteed by design

LOW VOLTAGE DIFFERENTIAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Differential Mode Termination Resistance	Rdm	100		110	Ohms	
Common Mode Termination Resistance	Rcm	110		190	Ohms	
Differential Mode Bias	Vdm	100		125	mV	All lines open
Common Mode Bias	Vcm	1.125		1.375	V	

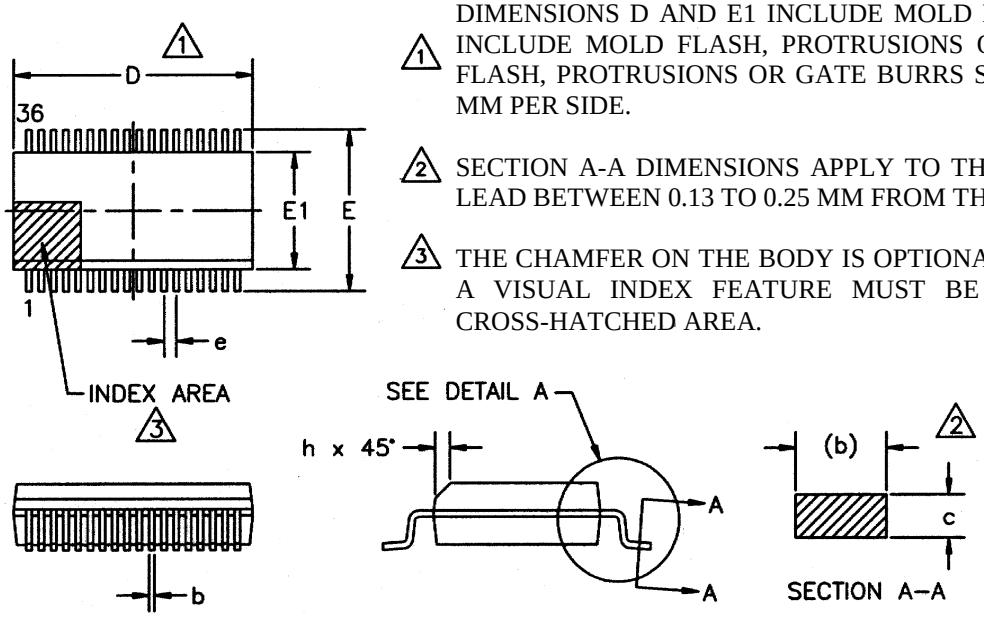
DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Current	I_{tpmr}		35		mA	All lines open
Input Leakage High	I_{ih}	-1.0			µA	
Input Leakage Low	I_{il}			1.0	µA	
Output Current High	I_{oh}	-1.0			mA	V_{OUT} = 2.4 volts; SE/LVD/ HVD pins only
Output Current Low	I_{ol}	4.0			mA	V_{OUT} = 0.4 volts; SE/LVD/ HVD pins only
DIFFSENS SE Operating Range	V_{seor}	-0.3		0.5	V	
DIFFSENS LVD Operating Range	V_{lvdor}	0.7		1.9	V	
DIFFSENS HVD Operating Range	V_{hvdor}	2.4		V_{tpwr} + 0.3	V	
DIFFSENSE Driver Output Voltage	V_{dso}	1.2		1.4	V	MSTR/ SLV=1; I_{ds}=0-5 mA
DIFFSENSE Driver Source Current	I_{dsh}		5	15	mA	MSTR/ SLV=1; V_{dso}=0V
DIFFSENSE Driver Sink Current	I_{dsl}	20		200	µA	MSTR/ SLV=1; V_{dso}=2.75V

REGULATOR CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Line Regulation	LI_{REG}		1.0	2.0	%	
Load Regulation	LO_{REG}		1.3	3.0	%	
Current Limit	I_{LIM}		350		mA	
Sink Current	I_{SINK}	200			mA	

DS2118M 36-PIN SSOP PACKAGE

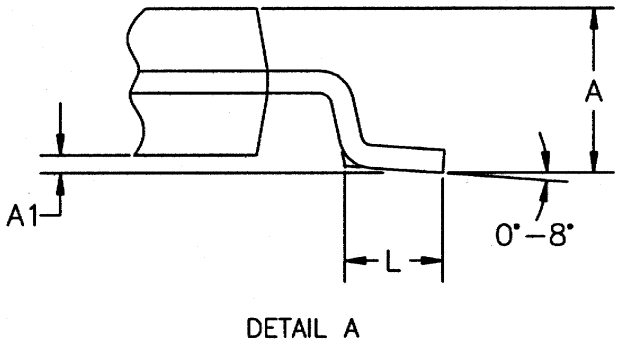


1 DIMENSIONS D AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.254 MM PER SIDE.

2 SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.13 TO 0.25 MM FROM THE LEAD TIP.

3 THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

DIM	MIN	MAX
A	2.44	2.64
A1	0.12	-
b	0.29	0.43
c	0.23	0.32
D	15.20	15.54
E	10.11	10.52
E1	7.40	7.60
e	0.80 BSC	
h	0.25	0.71
L	0.51	1.02



DIMENSIONS ARE IN MILLIMETERS